ABSTRACT

A method and apparatus are disclosed for staggering execution of an instruction. According to one embodiment of the invention, a macro instruction specifying an operation, and specifying a first and a second data operand in first and second registers, respectively, is received. The macro instruction is then split into a first micro instruction and a second micro instruction, the first micro instruction specifying the operation on a first corresponding segment including a first portion of the first data operand and a first portion of the second data operand, and the second micro instruction specifying the operation on a second corresponding segment including a second portion of the first data operand and a second portion of the second data operand. The first and second micro instructions are then executed.